Dealing with High-Speed Logic

WHEN ARE TRANSMISSION LINE TECHNIQUES NEEDED?

Much has been written about terminating PCB traces in their characteristic impedance, to avoid signal reflections. Tutorial MT-094 presents the basic design equations for microstrip and stripline transmission lines. However, it may not be clear when transmission line techniques are appropriate.

A good guideline to determine when the transmission line approach is necessary is as follows:

Terminate the transmission line in its characteristic impedance when the one-way propagation delay of the PCB track is equal to or greater than one-half the applied signal rise/fall time (whichever edge is faster).

For example, a 2 inch microstrip line over an $E_r = 4.0$ dielectric would have a delay of ~270 ps. Using the above rule strictly, termination would be appropriate whenever the signal rise time is < ~500 ps.

A more conservative rule is to use a 2 inch (PCB track length)/nanosecond (rise/fall time) rule. If the signal trace exceeds this trace-length/speed criterion, then termination should be used.

For example, PCB tracks for high-speed logic with rise/fall time of 5 ns should be terminated in their characteristic impedance if the track length is equal to or greater than 10 inches (where measured length *includes* meanders).

As an example of what can be expected today in modern systems, Figure 1 shows typical rise/fall times for several logic families including the SHARC DSPs operating on +3.3 V supplies. As would be expected, the rise/fall times are a function of load capacitance.

In the analog domain, it is important to note that this same 2 inch/nanosecond guideline should also be used with op amps and other circuits, to determine the need for transmission line techniques. For instance, if an amplifier must output a maximum frequency of f_{max}, then the equivalent risetime t_r is related to this f_{max}. This limiting risetime, t_r, can be calculated as:

$$t_r = 0.35/f_{max} \qquad \text{Eq. 1}$$

The maximum PCB track length is then calculated by multiplying t_r by 2 inch/nanosecond. For example, a maximum frequency of 100 MHz corresponds to a risetime of 3.5 ns, so a 7-inch or more track carrying this signal should be treated as a transmission line.

◆ **GaAs: 0.1ns**
◆ **ECL: 0.75ns**
◆ **ADI SHARC DSPs: 0.5 ns to 1 ns (Operating on +3.3V Supply)**
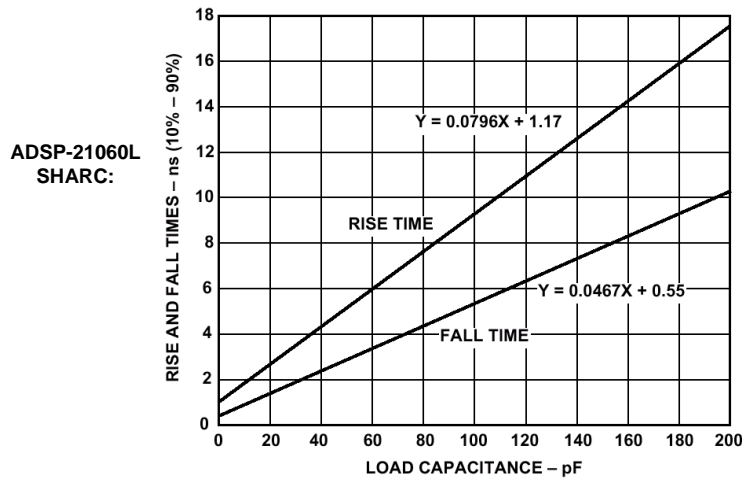
ADSP-21060L SHARC:

Figure 1: Typical DSP Output Rise Times and Fall Times

REDUCING THE EFFECT OF FAST LOGIC ON ANALOG CIRCUITS

The best ways to keep sensitive analog circuits from being affected by fast logic are to physically separate the two by the PCB layout, and to use no faster logic family than is dictated by system requirements. In some cases, this may require the use of several logic families in a system. An alternative is to use series resistance or ferrite beads to slow down the logic transitions where highest speed isn't required. Figure 2 shows two methods.
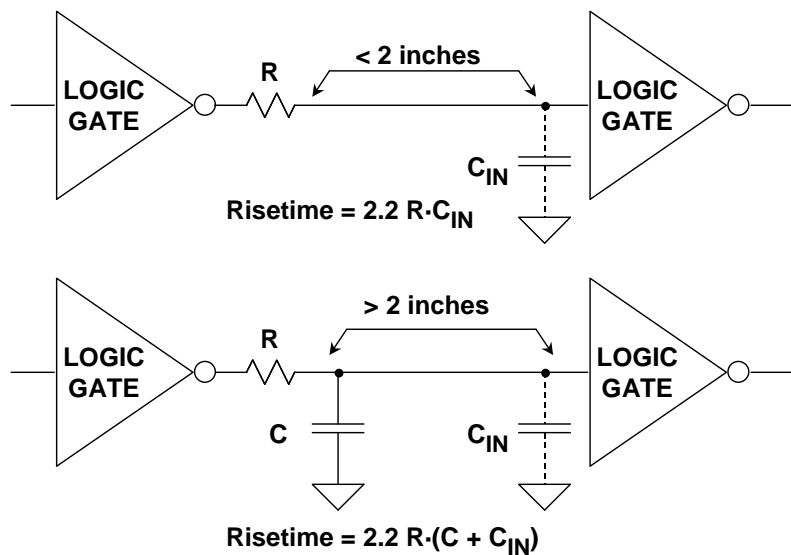

Figure 2: Damping Resistors Slow Down Fast Logic Edges to Minimize EMI/RFI Problems

In the first, the series resistance and the input capacitance of the gate form a lowpass filter. Typical CMOS input capacitance is 5 pF to 10 pF. Locate the series resistor close to the driving gate. The resistor minimizes transient currents and may eliminate the necessity of using transmission line techniques. The value of the resistor should be chosen such that the rise and fall times at the receiving gate are fast enough to meet system requirement, but no faster. Also, make sure that the resistor is not so large that the logic levels at the receiver are out of specification because of the voltage drop caused by the source and sink current which flow through the resistor. The second method is suitable for longer distances (>2 inches), where additional capacitance is added to slow down the edge speed. Notice that either one of these techniques increases delay and increases the rise/fall time of the original signal. This must be considered with respect to the overall timing budget, and the additional delay may not be acceptable.

Figure 3 shows a situation where several DSPs must connect to a single point, as would be the case when using read or write strobes bidirectionally connected from several DSPs. Small damping resistors shown in Figure 3A can minimize ringing provided the length of separation is less than about 2 inches. This method will also increase rise/fall times and propagation delay. If two groups of processors must be connected, a single resistor between the pairs of processors as shown in Figure 3B can serve to damp out ringing.
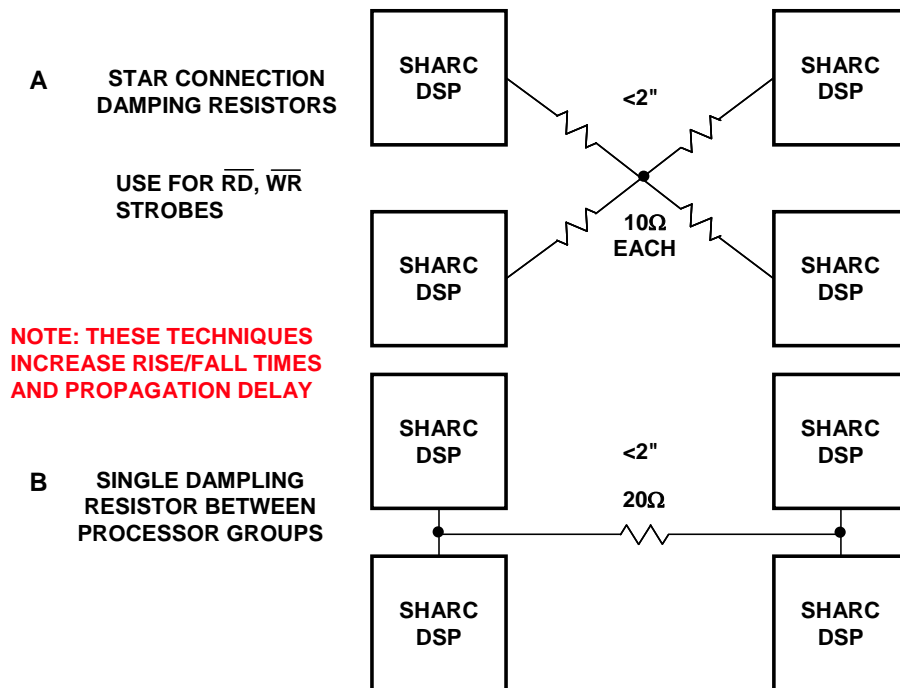

Figure 3: Series Damping Resistors for
High Speed DSP Interconnections

END TERMINATION AND SOURCE TERMINATION

The only way to preserve 1 ns or less rise/fall times over distances greater than about 2 inches without ringing is to use transmission line techniques. Figure 4 shows two popular methods of termination: end termination, and source termination. The end termination method (Figure 4A) terminates the cable at its terminating point in the characteristic impedance of the microstrip transmission line. Although higher impedances can be used, 50 Ω is popular because it minimizes the effects of the termination impedance mismatch due to the input capacitance of the terminating gate (usually 5 pF to 10 pF).
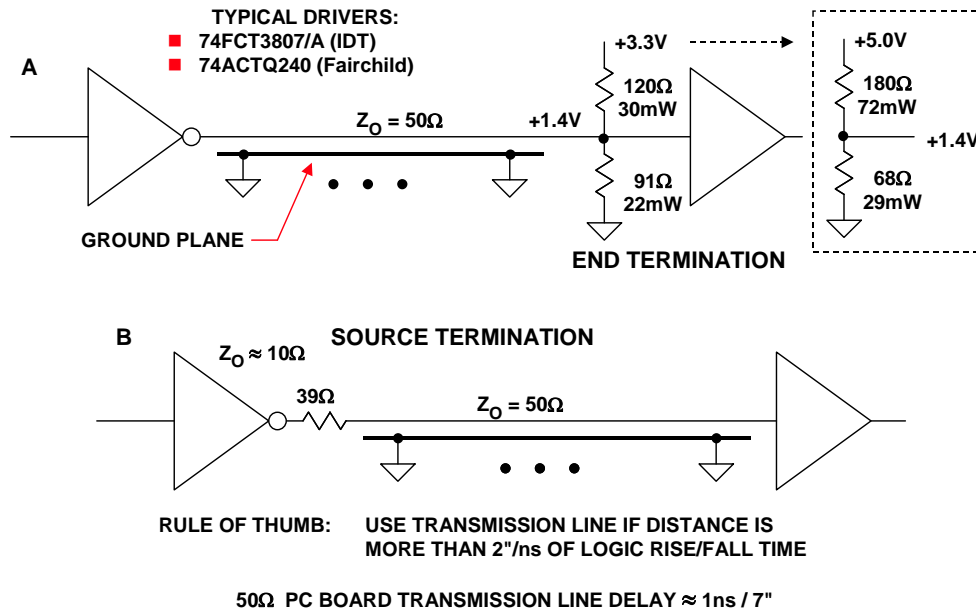

Figure 4: Termination Techniques for Controlled Impedance Microstrip Transmission Lines

In Figure 4A, the cable is terminated in a Thevenin impedance of 50 Ω terminated to +1.4 V (the midpoint of the input logic threshold of 0.8 V and 2.0 V). This requires two resistors (91 Ω and 120 Ω), which add about 50 mW to the total quiescent power dissipation to the circuit. Figure 4A also shows the resistor values for terminating with a +5 V supply (68 Ω and 180 Ω). Note that 3.3 V logic is much more desirable in line driver applications because of its symmetrical voltage swing, faster speed, and lower power. Drivers are available with less than 0.5 ns time skew, source and sink current capability greater than 25 mA, and rise/fall times of about 1 ns. Switching noise generated by 3.3 V logic is generally less than 5 V logic because of the reduced signal swings and lower transient currents.

The source termination method, shown in Figure 4B, absorbs the reflected waveform with an impedance equal to that of the transmission line. This requires about 39 Ω in series with the internal output impedance of the driver, which is generally about 10 Ω. This technique requires that the end of the transmission line be terminated in an open circuit, therefore no additional fanout is allowed. The source termination method adds no additional quiescent power dissipation to the circuit.

HIGH SPEED CLOCK DISTRIBUTION

Figure 5 shows a method for distributing a high speed clock to several devices. The problem with this approach is that there is a small amount of time skew between the clocks because of the propagation delay of the microstrip line (approximately 1 ns /7"). This time skew may be critical in some applications. It is important to keep the stub length to each device less than 0.5" in order to prevent mismatches along the transmission line.
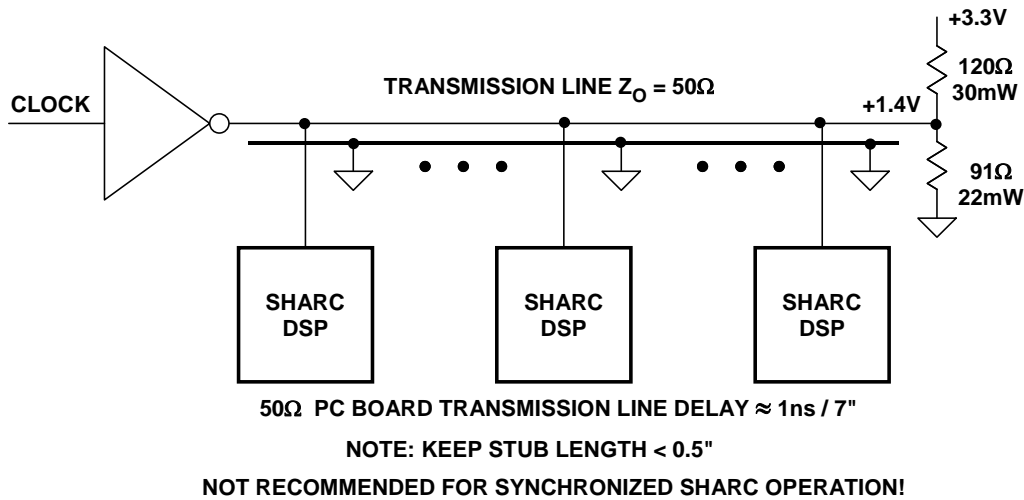
TRANSMISSION LINE $Z_O = 50\Omega$

CLOCK

+3.3V

120Ω
30mW

+1.4V

91Ω
22mW

SHARC
DSP

SHARC
DSP

SHARC
DSP

50Ω PC BOARD TRANSMISSION LINE DELAY ≈ 1ns / 7"

NOTE: KEEP STUB LENGTH < 0.5"

NOT RECOMMENDED FOR SYNCHRONIZED SHARC OPERATION!

Figure 5: Clock Distribution Using End-of-Line Termination

The clock distribution method shown in Figure 6 minimizes the clock skew to the receiving devices by using source terminations and making certain the length of each microstrip line is equal. There is no extra quiescent power dissipation as would be the case using end termination resistors.
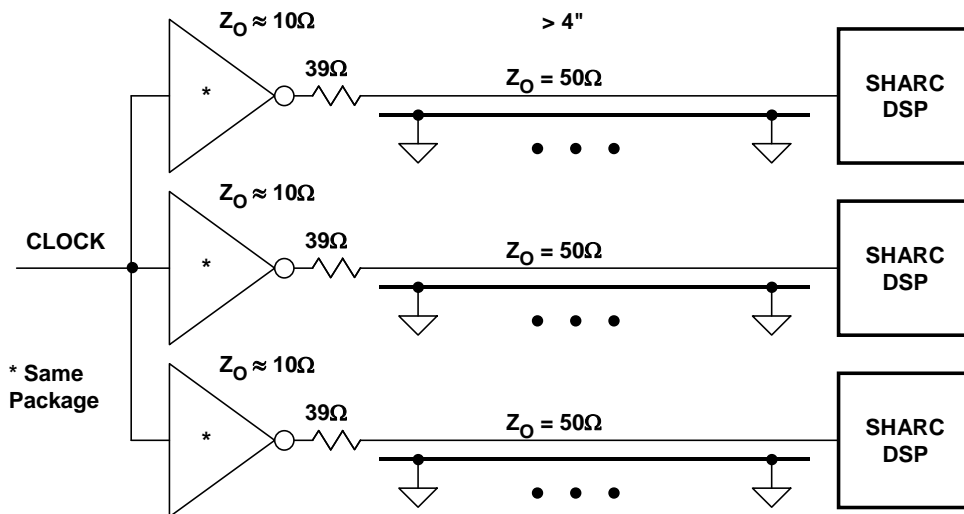
$Z_O \approx 10\Omega$

> 4"

39Ω

$Z_O = 50\Omega$

SHARC
DSP

$Z_O \approx 10\Omega$

CLOCK

39Ω

$Z_O = 50\Omega$

SHARC
DSP

* Same
Package

$Z_O \approx 10\Omega$

39Ω

$Z_O = 50\Omega$

SHARC
DSP

*Figure 6: Preferred Method of Clock Distribution
Using Source Terminated Transmission Lines*

TERMINATIONS IN BI-DIRECTIONAL LINKS

Figure 7 shows how source terminations can be used in bi-directional link port transmissions between SHARC DSPs. The output impedance of the SHARC driver is approximately 17 Ω, and therefore a 33-Ω series resistor is required on each end of the transmission line for proper source termination.

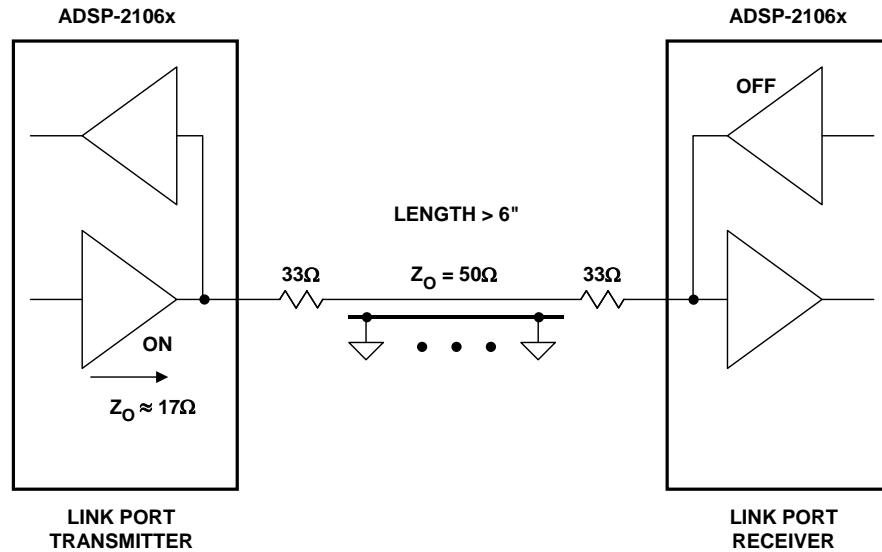**Figure 7: Source Termination for Bi-Directional
Transmission Between SHARC DSPs**

The method shown in Figure 8 can be used for bi-directional transmission of signals from several sources over a relatively long transmission line. In this case, the line is terminated at both ends, resulting in a dc load impedance of 25 Ω. SHARC drivers are capable of driving this load to valid logic levels.
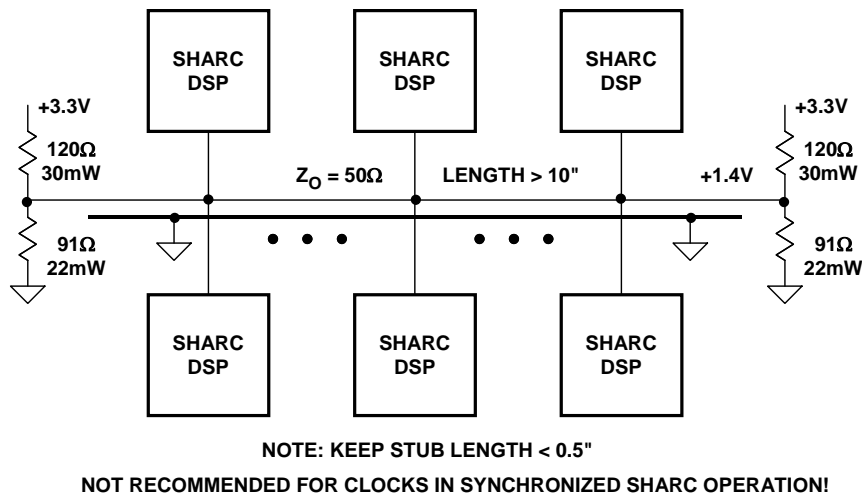

NOTE: KEEP STUB LENGTH < 0.5"

NOT RECOMMENDED FOR CLOCKS IN SYNCHRONIZED SHARC OPERATION!

Figure 8: Single Transmission Line Terminated at Both Ends

Emitter-coupled-logic (ECL) has long been known for low noise and its ability to drive terminated transmission lines with rise/fall times less than 2 ns. The family presents a constant load to the power supply, and the low-level differential outputs provide a high degree of common-mode rejection. However, ECL dissipates lots of power.

Recently, low-voltage-differential-signaling (LVDS) logic has attained widespread popularity because of similar characteristics, but with lower amplitudes and lower power dissipation than ECL. The defining LVDS specification can be found in Reference 1, and References 2 and 3 should also prove useful. The LVDS logic swing is typically 350 mV peak-to-peak centered about a common-mode voltage of +1.2 V. A typical driver and receiver configuration is shown in Figure 9. The driver consists of a nominal 3.5 mA current source with polarity switching provided by PMOS and NMOS transistors as in the case of the AD9430 12-bit, 170 /210 MSPS ADC. The output voltage of the driver is nominally 350 mV peak-to-peak at each output, and can vary between 247 mV and 454 mV. The output current can vary between 2.47 mA and 4.54 mA. The LVDS receiver is terminated in a 100 Ω line-to-line. According to the LVDS specification, the receiver must respond to signals as small as 100 mV, over a common-mode voltage range of 50 mV to +2.35 V. The wide common-mode receiver voltage range is to accommodate ground voltage differences up to ±1 V between the driver and receiver.
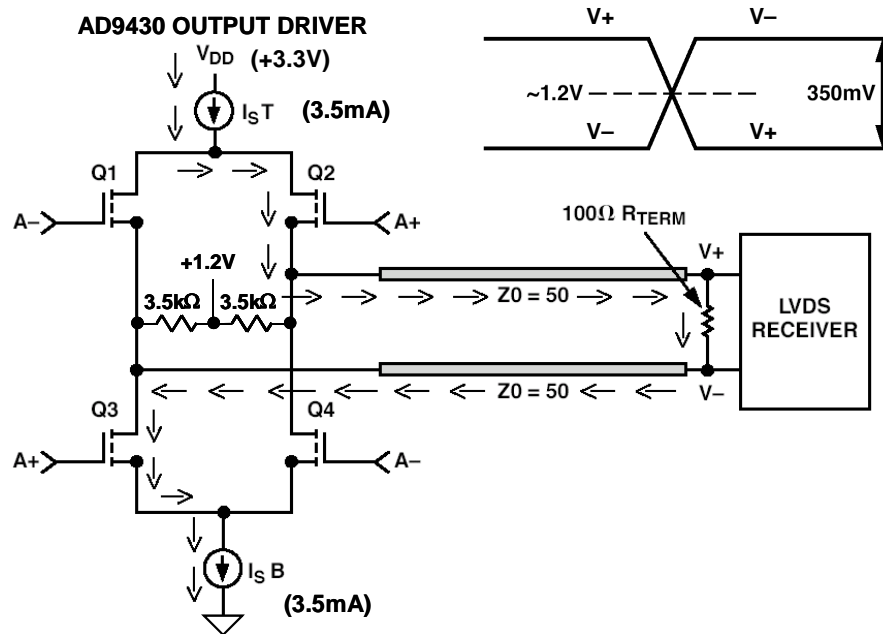

Figure 9: LVDS Driver and Receiver

The LVDS edge speed is defined as the 20% to 90% rise/fall time (as opposed to 10% to 90% for CMOS logic) and specified to be less than < 0.3 t_{ui}, where t_{ui} is the inverse of the data signaling rate. For a 210 MSPS sampling rate, t_{ui} = 4.76 ns, and the 20% to 80% rise/fall time must be less than $0.3 \times 4.76 = 1.43$ ns. For the AD9430, the rise/fall time is nominally 0.5 ns.

LVDS outputs for high-performance ADCs should be treated differently than standard LVDS outputs used in digital logic. While standard LVDS can drive 1 to 10 meters in high-speed digital

applications (dependent on data rate), it is not recommended to let a high-performance ADC drive that distance. It is recommended to keep the output trace lengths short (< 2 in.), minimizing the opportunity for any noise coupling onto the outputs from the adjacent circuitry, which may get back to the analog inputs. The differential output traces should be routed close together, maximizing common-mode rejection, with the 100 Ω termination resistor close to the receiver. Users should pay attention to PCB trace lengths to minimize any delay skew. A typical differential microstrip PCB trace cross section is shown in Figure 10 along with some recommended layout guidelines.
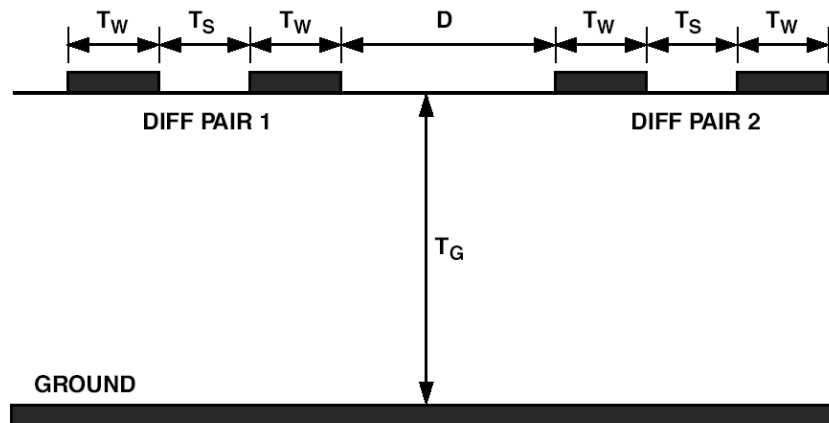
◆ Keep T_W, T_S, and D constant over the trace length
◆ Keep T_S ~ < $2T_W$
◆ Avoid use of vias if possible
◆ Keep D > $2T_S$
◆ Avoid 90° bends if possible
◆ Design T_W and T_G for ~ 50Ω

Figure 10: Microstrip PCB Layout for Two Pairs of LVDS Signals

LVDS also offers some benefits in reduced EMI. The EMI fields generated by the opposing LVDS currents tend to cancel each other (for matched edge rates). In high speed ADCs, LVDS offers simpler timing constraints compared to demultiplexed CMOS outputs at similar data rates. A demultiplexed data bus requires a synchronization signal that is not required in LVDS. In demuxed CMOS buses, a clock equal to one-half the ADC sample rate is needed, adding cost and complexity, that is not required in LVDS.

CLOCK GENERATION AND DISTRIBUTION PRODUCTS

Analog Devices offers ultra-low jitter clock distribution and clock generation products for wireless infrastructure, instrumentation, broadband, ATE and other applications demanding sub picosecond performance. ADI clock products are ideal for clocking high performance analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). ADI clock ICs integrate PLL cores, dividers, phase offset, skew adjust, and clock drivers in small chip scale packages.

REFERENCES:

1. TIA/EIA-644-A Standard, *Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits,* January 30, 2001.

2. IEEE Std. 1596.3-1996, *IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface,* IEEE, 1996.

3. Cindy Bloomingdale and Gary Hendrickson, "LVDS Data Outputs for High-Speed Analog-to-Digital Converter," Application Note AN-586, Analog Devices, 2002.

4. Hank Zumbahlen, *Basic Linear Design*, Analog Devices, 2006, ISBN: 0-915550-28-1. Also available as *Linear Circuit Design Handbook*, Elsevier-Newnes, 2008, ISBN-10: 0750687037, ISBN-13: 978-0750687034. Chapter 12

5. Walt Kester, *Analog-Digital Conversion,* Analog Devices, 2004, ISBN 0-916550-27-3, Chapter 9. Also available as *The Data Conversion Handbook*, Elsevier/Newnes, 2005, ISBN 0-7506-7841-0, Chapter 9.

6. Walter G. Jung, *Op Amp Applications*, Analog Devices, 2002, ISBN 0-916550-26-5, Chapter 7. Also available as *Op Amp Applications Handbook*, Elsevier/Newnes, 2005, ISBN 0-7506-7844-5. Chapter 7.